SPECIFICATION

Please replace the ABSTRACT with the following replacement ABSTRACT:

A biphase code detector and method for implementing the same. In accordance with one embodiment, the biphase code detector includes a receiver input for receiving a biphase encoded signal. The biphase encoded signal is a stream of unit bit cells each having a logic value encoded as a mid-bit transition between a first half-symbol signal component and a second half-symbol signal component. An integrated value is produced for ~~A demodulator demodulates~~ the first and the second half-symbol components of a received unit bit cell. The biphase code detector further includes a delta detector that generates a difference signal corresponding to the difference between the integrated ~~demodulated~~ values of the first and second half-symbol components to determine the logic value of the received unit bit cell. ~~In a preferred embodiment, the biphase code detector incorporates the delta detection function within an optimum receiver that integrates demodulation and detection functionality. For a given received signal energy, the biphase code detector of the present invention results in an approximate 3dB sensitivity increase in detector gain resulting in a lower probability of error and lower transmission power requirements.~~